REMARKS

In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all claims of the instant application are in condition for allowance, an indication of which is respectfully requested.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 2, 4, 12, and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 6,288,431 ("Iwasa") in view of U.S. Patent Number 4,996,574 ("Shirasaki") and U.S. Patent Number 4,356,211 ("Riseman"). Claims 6, 8, and 13 were rejected under § 103(a) as being unpatentable over Iwasa in view of Shirasaki and Riseman and further in view of U.S. Patent Number 7,163,851 ("Abadeer"). Claims 14, 16-18, and 20-22 were rejected under § 103(a) as being unpatentable over Iwasa in view of Riseman. Claim 15 was rejected under § 103(a) as being unpatentable over Iwasa in view of Riseman and further in view of U.S. Patent Number 6,770,516 ("Wu"). Claims 1-22 have been canceled without prejudice or disclaimer of subject matter, rendering their rejections moot.

New claims

Claims 23-42 have been added. New claim 23 recites a semiconductor device, comprising: a substrate, and a semiconductor region formed in a predetermined area of the substrate. The semiconductor region has a predetermined concentration of an impurity and a principal surface. In the semiconductor device, a first transistor having a semiconductor FIN structure and a second transistor having a planar structure are integrated in the semiconductor region.

The first transistor includes a trench region, source/drain regions each of which is formed so as to be buried in the trench region, and a semiconductor FIN structure. The semiconductor FIN structure is formed in the trench region so as to be buried in the trench region, and is located between the source/drain regions. The semiconductor FIN has a convex shape with an upper surface and second side surfaces. The first transistor also includes an isolation insulating film formed in the trench region so as to be buried between the source/drain regions and the first side surfaces of the trench region, and between the semiconductor FIN structure and the first side surfaces of the trench region. The first transistor also includes a gate insulating film disposed on the upper surface and both side surfaces of the semiconductor FIN structure, and, a gate electrode disposed on the second side surfaces and the upper surface of the semiconductor FIN structure with the gate insulating film interposed therebetween, and between the second side surfaces of the semiconductor FIN structure and the isolation insulating film.

The second transistor is formed on a part of the principal surface of the semiconductor region outside said trench region. The upper surface of the FIN structure of the first transistor does not protrude from the principal surface of the semiconductor region.

To provide context, the instant application relates to a three-dimensional structural transistor (e.g., a so called FINFET). Unlike a widely used known fabrication method in which a substrate is etched to form a FIN portion, in the instant application, a trench (e.g., a recess portion) is formed in a transistor formation region in a substrate. Thereafter, a FIN portion is grown in the recess portion. Thus, the FIN portion can be formed to protrude from an upper surface of the transistor formation region. As such, the FINFET according to the instant application can be integrated with a planar type transistor in a simple manner.

To this end, the instant application defines that an upper surface of a FIN structure of a first transistor does not protrude from a principal surface of the semiconductor region, and the first transistor and the second transistor having a planar structure are integrated on the semiconductor region. These features are not described or suggested by the cited prior art documents. That is, the cited prior art documents are not seen to show a semiconductor device that includes a first transistor having a semiconductor FIN structure and a second transistor having a planar structure, wherein the upper surface of the FIN structure of the first transistor does not protrude from the principal surface of the semiconductor region, as recited in claim 23.

For at least the foregoing reasons, Applicants respectfully request consideration and allowance of claim 23, along with its dependent claims.

Claim 26 recites a semiconductor device including a first transistor having a semiconductor FIN structure and a second transistor having a planar structure, wherein the upper surface of the FIN structure, the principal surface of the semiconductor region, an upper surface of each of the source/drain regions of the first transistor and an upper surface of each of the source/drain regions of the second transistor are located substantially at the same level. The cited prior art documents are not seen to describe or suggest these features of claim 26. Therefore, Applicants respectfully request consideration and allowance of claim 26, along with its dependent claims.

Conclusion

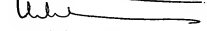
Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's

amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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